AMENDMENT

Amendments to the Claims

1. (currently amended) A process of forming a memory device, comprising:

forming a first topology over a substrate;

forming a first ferroelectric memory structure at the first topology and after forming the first topology; and

forming at least one subsequent ferroelectric memory structure over the first ferroelectric memory structure, wherein forming a first topology includes:

forming a first dielectric layer over the substrate;

forming a first metal layer over the first dielectric layer;

forming a second dielectric layer over the first metal layer;

forming a first electrode adjacent to the second dielectric layer;

forming a second metal layer over the second dielectric layer;

forming a third dielectric layer over the second metal layer;

forming a third metal layer over the third dielectric layer; and

forming a first filled via between the first metal layer and the second metal layer.

Claims 2-4 (cancelled)

5.(previously amended) The process according to claim 1, wherein forming a first ferroelectric memory structure further includes:

forming a first ferroelectric polymer memory layer over the first electrode; and

forming a second electrode over the first ferroelectric polymer memory layer.

6.(previously amended) The process according to claim 1, wherein forming a first ferroelectric memory structure and forming a subsequent ferroelectric memory structure further includes:

forming a first ferroelectric polymer memory layer over the first electrode;

forming a second electrode over the first ferroelectric polymer memory layer;

forming a second ferroelectric polymer memory layer over the second electrode; and

forming a third electrode over the second ferroelectric polymer memory layer.

Claims 7-29 (cancelled)

30.(previously added) A method, comprising:

forming a first electrode over a substrate;

forming a first ferroelectric oxide memory layer over the first electrode;

forming a second electrode over the first ferroelectric oxide memory layer; and

forming a second ferroelectric oxide memory layer over the first ferroelectric oxide memory layer, wherein the second ferroelectric oxide memory layer is larger than the first ferroelectric oxide memory layer.

31.(previously added) The method of claim 30, wherein the second ferroelectric oxide memory layer is formed so that a thickness of the first ferroelectric oxide memory layer is substantially equal to a thickness of the second ferroelectric oxide memory layer and so that a width of the second ferroelectric oxide memory layer is greater than a width of the first ferroelectric oxide memory layer.

32.(previously added) The method of claim 30, wherein forming the first ferroelectric oxide memory layer includes forming a ferroelectric oxide memory layer by chemical vapor deposition, spin-on deposition, or physical vapor deposition.

33.(previously added) The method of claim 30, the first electrode has a width that is a minimum feature of a photolithography technology, selected from 0.25 micron, 0.18 micron, 0.13 micron, and 0.11 micron.

34.(previously added) The method of claim 30, further comprising:

forming a via coupled to the first electrode prior to forming the first ferroelectric oxide memory layer.

35.(previously added) A method, comprising:

forming a structure having a cavity, wherein the structure is formed by:

forming a first electrode material over a substrate;

forming a first dielectric layer over the substrate and adjacent the first electrode material, wherein portions of the first electrode material and the first dielectric material define the cavity;

forming a via coupled to the first electrode; and

forming a first ferroelectric memory layer in the cavity over the first electrode material .

36.(previously added) The method of claim 35, wherein forming a first ferroelectric memory layer includes forming a first ferroelectric oxide memory layer in the cavity.

37.(previously added) The method of claim 35, wherein forming a first ferroelectric memory layer includes forming a first ferroelectric polymer memory layer in the cavity.

38.(previously added) The method of claim 35, wherein forming a first ferroelectric memory layer includes forming a first ferroelectric memory layer in the cavity after forming the via.

39.(currently amended) The method of claim 35, wherein forming a via includes forming a ~~tungsten~~ via filled with tungsten coupled to the first electrode.

40.(previously added) The method of claim 35, further comprising:

forming a second electrode material over the first ferroelectric memory layer; and

forming a second ferroelectric memory layer in the cavity and over the first ferroelectric memory layer, wherein a volume of the second ferroelectric memory layer is greater than a volume of the first ferroelectric memory material.

41.(previously added) The method of claim 40, further comprising:

forming a conductive layer over the second ferroelectric memory layer;

planarizing the conductive layer; and

patterning the conductive layer to form a third electrode; and

forming an interlayer dielectric (ILD) layer over the third electrode; and

forming a third ferroelectric memory layer over the interlayer dielectric layer.

42.(previously added). A method, comprising:

forming a structure having a cavity, wherein the structure includes at least one dielectric layer, at least one metal layer, and at least one via; and

forming at least one ferroelectric layer in the cavity.